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10/629,106	07/29/2003	Matthias Bonkabeta	2000.108300	6373

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EXAMINER	
VAN, LUAN V	
ART UNIT	PAPER NUMBER
1753	

DATE MAILED: 08/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,106	BONKABETA ET AL.	
	Examiner	Art Unit	
	Luan V. Van	1753	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 28 July 2006.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1,2,4-19,21-23,26,27,29-36,39-43 and 45 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,2,4-19,21-23,26,27,29-36,39-43 and 45 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's amendment of July 28, 2006 does not render the application allowable.

Status of Objections and Rejections

The rejection of claims 1, 2, 4-19, 21-23, 26, 27, 29-36, 39-43 and 45 under 35 U.S.C. 112, first paragraph, is withdrawn in view of Applicant's amendment.

All rejections from the previous office action are maintained.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 4-9, 14-15, 18, 19, 21-23, 26, 27, 29, 30, 35, 36, 39, 40, 43 and 45 are rejected under 35 U.S.C. 102(e) as being anticipated by Taylor '144.

Regarding claims 1, 4-5, 7, 9 and 14, Taylor '144 teaches a method of forming a layer of metal on a semiconductor structure, comprising: bringing an electrode into

contact with an electrolyte (claim 1 of Taylor '144); bringing said semiconductor structure into contact with said electrolyte (claim 1 of Taylor '144), said semiconductor structure comprising a plurality of openings having differing lateral widths (Fig. 1, column 3 lines 37-39); forming said layer of material to thereby overfill said plurality of openings (Fig. 1, profiles 1-3 overfills at least one of the openings) by applying in a first time interval a first current flowing from said electrode through said electrolyte to said semiconductor structure, said first current having a first amperage (profiles 1-3 of Fig. 1 is interpreted as the first amperage) comprising a plurality of first positive pulses (cathodic pulses, Fig. 1, profile 3), each of which are applied for first time duration, and a plurality of first negative pulses (anodic pulses, Fig. 1, profile 3), an integral of said first amperage over said first time interval having a first value greater than zero (Fig. 1, net deposition occurs in profiles 1-3), each of said plurality of first negative pulses being applied for a second time duration that is less than said first time duration (column 6 lines 4 - 7, see profile 3), an absolute value of the anodic pulse (first negative pulse) is less than the absolute value of the cathodic pulse (or first positive pulse, profiles 1-2 of Fig. 1), wherein said layer of material has an initial thickness above said semiconductor structure (Fig. 1, indicated by dash lines of profiles 1-3); and applying in a second time interval a second current flowing from said electrode through said electrolyte to said semiconductor structure, said second current having a second amperage (Fig. 1, profile 4) comprising a plurality of the second negative pulses, each of said plurality of second negative pulses having an absolute value that is greater than said absolute value of said plurality of first negative pulses (anodic pulses in profile 4 is lower than the anodic

pulses in profiles 1-3 of Fig. 1), an integral of said second amperage over said second time interval having a second value less than zero (Fig. 1, profile 4 is completely anodic).

Regarding claim 2, Taylor '144 teaches "the cathodic-to-anodic <u>net charge ratio</u> will be <u>greater than one</u>, in order to provide a net deposition of metal on the surface" (column 5 lines 15-23). An absolute of said first value is greater than an absolute of said second value, since there is a net deposition of metal on the surface.

Regarding claims 6 and 8, Taylor '144 teaches pulses have a substantially rectangular shape (Fig. 1).

Regarding claim 15, Taylor '144 teaches a thin conducting layer (ie, seed layer) is deposited over the entire surface of the element to provide electrical conductivity for the electroplating step (column 3 lines 45-57).

Regarding claim 18, Taylor '144 teaches chemical mechanical polishing said semiconductor structure (example 1).

Regarding claims 19 and 39, Taylor '144 teaches a method, comprising: providing a semiconductor structure comprising a plurality of openings having different lateral widths (column 3 lines 35-45); electroplating said semiconductor structure to deposit a layer of metal on said semiconductor structure and thereby overfill said plurality of openings (column 3 lines 35-45) with said metal, wherein said electroplating process is formed by applying in a first time interval (Fig. 1, profiles 1-3) a first current flowing from an electrode through an electrolyte to said semiconductor structure, said first current having a first amperage comprising a plurality of first positive pulses (any

cathodic pulses in profiles 1-3, Fig. 1) and a plurality of first negative pulses (any anodic pulses in profiles 1-3, Fig. 1), an integral of said first amperage over said first time interval having a first value greater than zero (column 5 lines 15-23, net deposition occurs in profiles 1-3), wherein said layer of material has an initial thickness above said semiconductor structure (Fig. 1, indicated by dash lines of profiles 1-3); after performing said electroplating process, reducing said the initial thickness of said layer of metal by electropolishing said semiconductor structure for preferentially removing said metal from said at least one elevation (Fig. 1, profile 4), wherein said electropolishing process is formed by applying in a second time interval (Fig. 1, profiles 4) a second current flowing from an electrode through an electrolyte to said semiconductor structure, said second current having a second amperage comprising a plurality of second negative pulses (anodic pulses in profiles 4, Fig. 1), each of said plurality of second negative pulses having an absolute value that is greater than an absolute value of said plurality of first negative pulses (anodic pulses in profile 4 is more anodic or negative than the anodic pulses in profiles 1-3, Fig. 1), an integral of said second amperage over said second time interval having a second value less than zero (Fig. 1, profile 4 is completely anodic); and after performing said electropolishing process, performing a chemical mechanical polishing said semiconductor structure, said chemical mechanical polishing removing a surplus of said metal from said at least one elevation and planarizing a surface of said semiconductor structure (example 1).

Regarding claims 21-23, 27, 29, and 35-36 Taylor '144 teaches a method of forming a layer of metal on a semiconductor structure, comprising: bringing an electrode

into contact with an electrolyte (claim 1); bringing said semiconductor structure into contact with said electrolyte (claim 1); wherein said electroplating is performed by applying in a first time interval a first current flowing from said electrode through said electrolyte to said semiconductor structure, said first current having a first amperage comprising a plurality of first positive pulses and a plurality of first negative pulses, an integral of said first amperage over said first time interval having a first value greater than zero (Fig. 1, profiles 1-3); and wherein said electropolishing is perforned by applying in a second time interval a second current flowing from said electrode through said electrolyte to said semiconductor structure, said second current having a second amperage, an integral of said second amperage over said second time interval having a second value less than zero (Fig. 1, profiles 1-4).

Regarding claims 26 and 30, Taylor '144 teaches the pulses have a substantially rectangular shape (Fig. 1).

Regarding claim 40, Taylor '144 teaches a thin conducting layer (ie, seed layer) is deposited over the entire surface of the element to provide electrical conductivity for the electroplating step (column 3 lines 45-57).

Regarding claims 43 and 45 Taylor '144 teaches electroplating on a semiconductor structure for increasing a thickness of a metal layer (Fig. 1, profiles 2-3); and electroplating is performed after electropolishing (Fig. 1, profile 1-3). Further, electropolishing is performed after electroplating (Fig. 1, profile 1-4).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 2, 4-9 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor '144, assuming only profile 3 of Fig. 1 is the first amperage.

Regarding claims 1, 4-5, 7, 9 and 14, Taylor '144 teaches a method of forming a layer of metal on a semiconductor structure, comprising: bringing an electrode into contact with an electrolyte (claim 1 of Taylor '144); bringing said semiconductor structure into contact with said electrolyte (claim 1 of Taylor '144), said semiconductor structure comprising a plurality of openings having differing lateral widths (Fig. 1, column 3 lines 37-39); applying in a first time interval a first current flowing from said electrode through said electrolyte to said semiconductor structure, said first current having a first amperage comprising a plurality of first positive pulses (cathodic pulses, Fig. 1, profile 3), each of which are applied for first time duration, and a plurality of first negative pulses (anodic pulses, Fig. 1, profile 3), an integral of said first amperage over

said first time interval having a first value greater than zero (Fig. 1, net deposition occurs in profile 3), each of said plurality of first negative pulses the apply for second time duration that is less than said first time duration (column 6 lines 4 - 7), wherein said layer of material has an initial thickness above said semiconductor structure (Fig. 1, indicated by dash lines of profiles 1-3); and reducing said initial thickness of said layer by applying in a second time interval a second current flowing from said electrode through said electrolyte to said semiconductor structure, said second current having a second amperage (Fig. 1, profile 4) comprising a plurality of the second negative pulses, each of said plurality of second negative pulses having an absolute value that is greater than said absolute value of said plurality of first negative pulses (anodic pulses in profile 4 is lower than the anodic pulses in profile 3 of Fig. 1), an integral of said second amperage over said second time interval having a second value less than zero (Fig. 1, profile 4 is completely negative).

The reference to Taylor '144 differs from the instant claims in that the absolute value of the anodic pulse (first negative pulse) is about equal to the absolute value of the cathodic pulse (or first positive pulse) in profile 3 of Fig. 1. However, Taylor '144 teach that the absolute value of the anodic pulse (first negative pulse) can be less than the absolute value of the cathodic pulse (or first positive pulse) as shown in profiles 1 and 2 of Fig. 1; and that "the peak currents of the anodic and cathodic pulses are adjusted to provide a cathodic/anodic charge transfer ratio that [is] greater than one" (column 4 lines 49-51).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method of Taylor '144 by modifying the peak currents such that the absolute value of the anodic pulse (first negative pulse) is less than the absolute value of the cathodic pulse (or first positive pulse) in order to produce a uniform and complete filling of the recesses with metal (column 2 lines 39-44).

Regarding claim 2, Taylor '144 teaches "the cathodic-to-anodic net charge ratio will be greater than one, in order to provide a net deposition of metal on the surface" (column 5 lines 15-23). An absolute of said first value is greater than an absolute of said second value, since there is a net deposition of metal on the surface.

Regarding claims 6 and 8, Taylor '144 teaches pulses have a substantially rectangular shape (Fig. 1).

Regarding claim 15, Taylor '144 teaches a thin conducting layer (ie, seed layer) is deposited over the entire surface of the element to provide electrical conductivity for the electroplating step (column 3 lines 45-57).

Regarding claim 18, Taylor '144 teaches chemical mechanical polishing said semiconductor structure (example 1).

Claims 10-13 and 31-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor '144 in view of Piersol.

Taylor '144 teach the method as described above in addressing claims 1 and 19-20. The difference between the reference to Taylor '144 and the instant claims is that the reference does not explicitly teach using sinusoidal waveform.

However, using sinusoidal waveform for electroplating is well known in the art. For example, Piersol teach that by using sinusoidal waveform, "the rate of evolution of hydrogen is varied frequently and suddenly, and the gradual accumulation of hydrogen at the cathode surface is obviated. The troublesome sudden variations in plating conditions caused by such accumulations are likewise obviated" (pg. 2 lines 88-95).

Furthermore, modifying the parameters of a sinusoidal waveform to match the basic shape of a rectangular waveform would inherently yield the same expected plating or deplating effect--the only difference being that the current change is continuous rather than discreet.

Relevant to claims 10-11, the condition when the offset is greater than zero and wherein an absolute of the amplitude is greater than an absolute of the offset would result in a net deposition of metal on the surface, since "the cathodic-to-anodic net charge ratio will be greater than one" (Fig. 1, profiles 1-3).

Relevant to claims 12 and 33, the condition when the offset is less than zero would result in a net removal of metal on the surface (Fig. 1, profile 4).

Relevant to claims 13, 32 and 34, the condition when an absolute of the amplitude is equal to an absolute of the offset is equivalent to applying a DC current--as purely cathodic when the offset is greater than zero, or purely anodic when the offset is less than zero (Fig. 1, profile 4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Taylor '144 by using sinusoidal waveform for electroplating as taught by Piersol, because it would prevent the gradual

accumulation of hydrogen at the cathode surface. Furthermore, it is within the ability to one having ordinary skill in the art to modify the parameters of a sinusoidal waveform in order to achieve the same expected plating or deplating effect as compared to that from a rectangular waveform.

Claims 16-17 and 41-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor '144 in view of Taylor et al. '528.

Taylor '144 teach the method as described above in addressing claims 1-9, 14-15, 18-30, 35-40, and 43-46.

The difference between the reference to Taylor '144 and the instant claims is that the reference does not explicitly teach depositing an electrically conductive seed layer by physical vapor deposition nor electroless plating.

Taylor et al. '528 teach that "in order to prepare for the deposition of the copper layer, the surfaces to be plated, e.g., the surfaces...the interior surfaces of the vias...and the inside of the through-hole...are covered with a <u>thin layer of a conductor</u> by conventional procedures, e.g., by <u>sputtering</u>, <u>electroless deposition</u>, or the like" (column 9 lines 45-50).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Taylor '144 by using depositing the seed layer by physical vapor deposition (which is a form of sputtering) or electroless plating as taught by Taylor et al. '528, because depositing by physical vapor deposition and electroless plating is conventionally known, and because depositing the seed layer by

physical vapor deposition or electroless plating forms a conformal layer in order to initiate the deposition of the copper layer and to deposit the copper layer uniformly.

Response to Arguments

Applicant's arguments have been fully considered but they are not persuasive.

In the arguments presented on page 14-15 of the amendment, the applicant argues that Taylor '144 do not anticipate the pending claims by elaborating that the pending claims recite the formation of a layer of material during the first time interval, and reducing the thickness of the layer of material during a second time interval. The examiner respectfully disagrees. In the 102(e) rejection, the first time interval of Taylor '144 comprises the electroplating profiles I-III and the second time interval comprises profile IV. Since the first time interval of Taylor '144 overfills the plurality of openings that have different lateral widths (see Fig. 1), Taylor '144 anticipates the pending claims.

The applicant further argues that Taylor '144 teach that the smaller features are typically filled first and the larger features are fill in one or more subsequent steps. The examiner acknowledges that this statement is accurate. However, the smaller features can have different lateral widths as shown by the two smaller features in Fig. 1. Each of the electroplating profiles II-III of Taylor '144 overfills the two smaller features having different lateral widths. Therefore, Taylor '144 anticipates the pending claims.

On pages 15-16, the applicant argues that Taylor '144 does not teach that the negative pulses during the first time period is less than the duration of the positive pulses during the first time period. The examiner agrees that this is true for profiles I

and II. However, this is not true for profile III as shown in Fig. 1. In profile III the negative pulses is less than the duration of the positive pulses. Because the first time interval of Taylor '144 comprises the electroplating profiles I-III, Taylor '144 anticipates the pending claims. Furthermore, since the pending claims recite "comprising", profiles I and II can be included in the first time interval.

On page 16, the applicant argues that "neither profile I or II overfill the plurality of openings of differing widths." The examiner respectfully disagrees. Taylor '144 clearly shows that profile II in Fig. 1 overfills the two smaller features having different lateral widths.

Finally, the applicant argues that profile III of Taylor '144 is not appropriate for filling smaller openings. However, the arguments of counsel cannot take the place of evidence in the record. *In re Schulze*, 346 F.2d 600, 602, 145 USPQ 716, 718 (CCPA 1965). Objective evidence which must be factually supported by an appropriate affidavit or declaration to be of probative value includes evidence of unexpected results, commercial success, solution of a long-felt need, inoperability of the prior art, invention before the date of the reference, and allegations that the author(s) of the prior art derived the disclosed subject matter from the applicant. See, for example, *In re De Blauwe*, 736 F.2d 699, 705, 222 USPQ 191, 196 (Fed. Cir. 1984). See MPEP 716.01(c).

Conclusion

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan V. Van whose telephone number is 571-272-8521. The examiner can normally be reached on M-F 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam Nguyen can be reached on 571-272-1342. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LVV
August 18, 2006

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